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net and system data-flow **subgraphs**, in order to identify ... cation is to be **integrated** in allocation as well as **scheduling** ... needed when **common** subcomponents shall be shared. Task ... and assigned component data-flow graph, **CFG** ..... Particularly, the optimal **circuit** in relation to the area delay ...  
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lication-specific **integrated circuit** (ASIC)]. As new processor architectures are ..... When translating assembly codes from DSPs, it is **common** to encounter highly pipelined software ..... the **subgraph** (CFG). Successive predicates form conjunctions. .... directed **scheduling** [41]. **ASAP** and **ALAP** **scheduling** gener- ...  
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scale **integrated** (VLSI) **circuits** become more and more important in the design ..... Some systems separate DFG and **CFG**, others just combine both graphs. ... execution path or operation can be detected by traversing the **subgraph** between ..... Both the **ASAP** and **ALAP** **scheduling** approaches stem out from unlimited ...  
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**ASAP** and **ALAP** **scheduling** algorithms to determine the range of control steps ..... Several **scheduling** techniques based on a control flow graph (**CFG**) model are ... for each variable in the loop, thus, resulting in a complex **sub graph** with a .... Today, Very High Speed

**Integrated Circuit(VHSIC) Hardware Description ...**[citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.99.1037&rep=rep1](http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.99.1037&rep=rep1)**[PDF] EMBEDDED** systems are dedicated to an application do-

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a **common** approach in the design of embedded systems is to implement the control-dominated ... custom hardware, in application-specific **integrated-circuit** or field-programmable gate-array ..... **subgraphs**. Finally, we apply standard Trimaran **scheduling** and ..... **ASAP**, Steamboat Springs, CO, Sep. 2006, pp. 39-44. ...

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plexity of silicon-**integrated circuits** proceeds according to ..... For the **CFG** and DFG some **common** basic properties ..... (**ASAP**) driven, in other words, it is the simplest list scheduling-... execution time instead of rescheduling the task **subgraph**. By ... tended for combined retiming, **scheduling**, and partitioning ...

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maps high-level parallel C language descriptions into **circuit**- level netlists targeted to FPGAs. ... eral composed of three **subgraphs**, called the init, subinit and body graphs. .... that the **schedule** in the body graph is p2D1E to accommo- ..... application representation, we **integrated** our findings seam- ...

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